

L1 35978 S 395/?/CCLS
L2 29 S L1 AND (SINGLE (1A) CHIP (5A) PROCESSOR?)/AB
L3 0 S L2 AND (VARIABLE (5A) SPEED (5A) CLOCK?)
L4 16 S L1 AND (VARIABLE (3A) SPEED (5A) CLOCK?)
L5 369 S L1 AND (SINGLE (2A) CHIP (5A) PROCESSOR?)
L6 0 S L4 AND L5
L7 289 S L1 AND (VARIABLE (5A) CLOCK?)
L8 11 S L5 AND L7
L9 25 S L1 AND (PROCESSOR? AND CLOCK? AND CHIP?)/AB
L10 218 S L1 AND (PROCESSOR? AND CHIP?)/AB
L11 0 S L10 AND (VARIABLE (5A) CLOCK?)

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=> s 395/?/ccls
L1      35978 395/?/CCLS

=> s l1 and (single (1a) chip (5a) processor?)/ab
      83017 SINGLE/AB
      10969 CHIP/AB
      17446 PROCESSOR?/AB
      43 (SINGLE (1A) CHIP (5A) PROCESSOR?)/AB
L2      29 L1 AND (SINGLE (1A) CHIP (5A) PROCESSOR?)/AB

=> s l2 and (variable (5a) speed (5a) clock?)
      292127 VARIABLE
      520828 SPEED
      258622 CLOCK?
      143 VARIABLE (5A) SPEED (5A) CLOCK?
L3      0 L2 AND (VARIABLE (5A) SPEED (5A) CLOCK?)

=> s l1 and (variable (3a) speed (5a) clock?)
      292127 VARIABLE
      520828 SPEED
      258622 CLOCK?
      119 VARIABLE (3A) SPEED (5A) CLOCK?
L4      16 L1 AND (VARIABLE (3A) SPEED (5A) CLOCK?)

=> s l1 and (single (2a) chip (5a) processor?)
      890378 SINGLE
      84891 CHIP
      99027 PROCESSOR?
      714 SINGLE (2A) CHIP (5A) PROCESSOR?
L5      369 L1 AND (SINGLE (2A) CHIP (5A) PROCESSOR?)

=> s l4 and l5
L6      0 L4 AND L5

=> s l1 and (variable (5a) clock?)
      292127 VARIABLE
      258622 CLOCK?
      2969 VARIABLE (5A) CLOCK?
L7      289 L1 AND (VARIABLE (5A) CLOCK?)

=> s l5 and l7
L8      11 L5 AND L7

=> d l8 kwic 1-11

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US PAT NO: 5,615,402 [IMAGE AVAILABLE] L8: 1 of 11
 US-CL-CURRENT: 395/800; 364/704, 736, 748; 395/250, 410, 467

DETDESC:

DETD(27)

The EX stages, EXX and EXY, perform the operations defined by the instruction. Instructions spend a variable number of clocks in EX, i.e., they are allowed to execute out of order (out of order completion). Both EX stages include adder, . . .

DETDDESC:

DETD(36)

Referring to FIG. 2, for the exemplary embodiment, microprocessor 10 is used in a processor system that includes a single chip memory and bus controller 82. The memory/bus controller 82 provides the interface between the microprocessor and the external memory subsystem--level. . .

US PAT NO: 5,611,071 [IMAGE AVAILABLE] L8: 2 of 11
US-CL-CURRENT: 395/460, 307, 403, 470, 471, 473, 496, 855

DETDDESC:

DETD(48)

The execution stages EXX and EXY perform the operations defined by the instruction. Instructions spend a variable number of clocks in EX, i.e., they are allowed to execute out of order (out of order completion). Both EX stages include adder,. . .

DETDDESC:

DETD(52)

Referring to FIG. 2, for the exemplary embodiment, microprocessor 10 is used in a processor system that includes a single chip memory and bus controller 82. The memory/bus controller 82 provides the interface between the microprocessor and the external memory subsystem--level. . .

US PAT NO: 5,596,740 [IMAGE AVAILABLE] L8: 3 of 11
US-CL-CURRENT: 395/484; 364/DIG.1, DIG.2; 365/189.02, 230.02, 230.03; 395/454

DETDDESC:

DETD(32)

The execution stages EXX and EXY perform the operations defined by the instruction. Instructions spend a variable number of clocks in EX, i.e., they are allowed to execute out of order (out of order completion). Both EX stages include adder,. . .

DETDDESC:

DETD(34)

Referring to FIG. 2, for the exemplary embodiment, microprocessor 10 is used in a processor system that includes a single chip memory and bus controller 82. The memory/bus controller 82 provides the interface between the microprocessor and the external memory subsystem--level. . .

US PAT NO: 5,596,731 [IMAGE AVAILABLE] L8: 4 of 11
US-CL-CURRENT: 395/309, 449, 855

DETDDESC:

DETD(33)

The execution stages EXX and EXY perform the operations defined by the instruction. Instructions spend a variable number of clocks in EK i.e.,

they are allowed to execute out of order (out of order completion). Both EX stages include adder, . . .

DETDESC:

DETD(36)

Referring to FIG. 2, for the exemplary embodiment, microprocessor 10 is used in a processor system that includes a single chip memory and bus controller 82. The memory/bus controller 82 provides the interface between the microprocessor and the external memory subsystem--level. . . .

US PAT NO: 5,584,009 [IMAGE AVAILABLE] L8: 5 of 11
US-CL-CURRENT: 395/444; 364/261.5, 261.7, DIG.1; 395/445, 449, 464

DETDESC:

DETD(27)

The execution stages EXX and EXY perform the operations defined by the instruction. Instructions spend a variable number of clocks in EX, i.e., they are allowed to execute out of order (out of order completion). Both EX stages include adder, . . .

DETDESC:

DETD(36)

Referring to FIG. 2, for the exemplary embodiment, microprocessor 80 is used in a processor system that includes a single chip memory and bus controller 82. The memory/bus controller 82 provides the interface between the microprocessor and the external memory subsystem--level. . . .

US PAT NO: 5,471,598 [IMAGE AVAILABLE] L8: 6 of 11
US-CL-CURRENT: 395/449; 364/231.8, 243.4, 243.41, 964, 964.2, DIG.1, DIG.2;
395/394, 465, 467, 496, 800

DETDESC:

DETD(27)

The execution stages EXX and EXY perform the operations defined by the instruction. Instructions spend a variable number of clocks in EX, i.e., they are allowed to execute out of order (out of order completion). Both EX stages include adder, . . .

DETDESC:

DETD(36)

Referring to FIG. 2, for the exemplary embodiment, microprocessor 80 is used in a processor system that includes a single chip memory and bus controller 82. The memory/bus controller 82 provides the interface between the microprocessor and the external memory subsystem--level. . . .

US PAT NO: 5,428,746 [IMAGE AVAILABLE] L8: 7 of 11
US-CL-CURRENT: 395/306; 364/925.6, 926.92, 926.93, DIG.2; 395/280, 800

CLAIMS:

CLMS(10)

10. A processor formed on a single integrated circuit chip, comprising:
means receiving a fixed frequency clock signal for providing an internal
clock signal and a variable frequency clock signal, said variable
frequency clock signal having a frequency set by a first control signal
that is less than that of said internal clock signal,
means . . . a plurality of protocols designated by said second control
signal, said input-output timing signal generating means being operated
from said variable frequency clock signal,
means responsive to a memory device read or write instruction decoded by
said decoding means for generating memory address strobe. . .

US PAT NO: 5,341,470 [IMAGE AVAILABLE]

L8: 8 of 11

US-CL-CURRENT: 345/185; 395/509

DETDESC:

DETD(82)

One of the reasons why so much imaging capability is available under the
system shown is that the single chip 5200 contains several processors
working in parallel together with several memories, all accessible under a
crossbar switch which allows for substantially instantaneous rearrangement
of. . .

DETDESC:

DETD(97)

FIG. . . . BLANK-. Blanking for VGA is given a fixed switch-selected
delay in circuit 4321. Blanking BLANK- passes through a 0-32 dot clock
period mode dependent variable delay circuit 4322 followed by the delay in
circuit 4321. The sync signals VSYNC- and HSYNC- are delayed by a. . .

DETDESC:

DETD(326)

Blanking . . . fixed delay F2 compensates for the circuit delays of the
LUT, other logic and digital to analog converters 4030. The variable delay
of 2N dot clocks recognizes that t
he selector circuit 4051 coacts with LUT
and DACs to process color codes according to different modes to. . .

US PAT NO: 5,309,551 [IMAGE AVAILABLE]

L8: 9 of 11

US-CL-CURRENT: 395/131; 345/199; 395/503, 509

DETDESC:

DETD(82)

One of the reasons why so much imaging capability is available under the
system shown is that the single chip 5200 contains several processors
working in parallel together with several memories, all accessible under a
crossbar switch which allows for substantially instantaneous rearrangement
of. . .

DETDESC:

DETD(97)

FIG. . . . BLANK-. Blanking for VGA is given a fixed switch-selected delay in circuit 4321. Blanking BLANK- passes through a 0-32 dot clock period mode dependent variable delay circuit 4322 followed by the delay in circuit 4321. The sync signals VSYNC- and HSYNC- are delayed by a. . .

DETD(DESC:

DETD(326)

Blanking . . . fixed delay F2 compensates for the circuit delays of the LUT, other logic and digital to analog converters 4030. The variable delay of 2N dot clocks recognizes that the selector circuit 4051 coacts with LUT and DACs to process color codes according to different modes to. . .

US PAT NO: 5,293,468 [IMAGE AVAILABLE] L8: 10 of 11
US-CL-CURRENT: 395/131, 501

DETD(DESC:

DETD(83)

One of the reasons why so much imaging capability is available under the system shown is that the single chip 5200 contains several processors working in parallel together with several memories, all accessible under a crossbar switch which allows for substantially instantaneous rearrangement of. . .

DETD(DESC:

DETD(98)

FIG. . . . BLANK-. Blanking for VGA is given a fixed switch-selected delay in circuit 4321. Blanking BLANK- passes through a 0-32 dot clock period mode dependent variable delay circuit 4322 followed by the delay in circuit 4321. The sync signals VSYNC- and HSYNC- are delayed by a. . .

DETD(DESC:

DETD(325)

Blanking . . . fixed delay F2 compensates for the circuit delays of the LUT, other logic and digital to analog converters 4030. The variable delay of 2N dot clocks recognizes that the selector circuit 4051 coacts with LUT and DACs to process color codes according to different modes to. . .

CLAIMS:

CLMS(7)

7. The palette device of claim 1 wherein the palette device includes a clock control circuit supplying clock pulses, and said variable delay circuit includes a series of flip-flops clocked by said clock pulses from said clock control circuit, the series of. . .

US PAT NO: 4,989,133 [IMAGE AVAILABLE] L8: 11 of 11
US-CL-CURRENT: 395/672; 364/242.6, 242.8, 245.5, 245.9, 247, 247.8, 254,

254.6, 271, 271.3, 280, 281.3, 281.4, 281.8, DIG.1; 395/680

DETDESC:

DETD(2)

The microcomputer described in this example comprises an integrated circuit device in the form of a single silicon chip having both a processor and memory in the form of RAM as well as links to permit external communication. The main elements of the. . .

DETDESC:

DETD(137)

assigns the current value of the processor's clock to the variable. A "timer" input is represented as

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L2 29 S L1 AND (SINGLE (1A) CHIP (5A) PROCESSOR?)/AB
L3 0 S L2 AND (VARIABLE (5A) SPEED (5A) CLOCK?)
L4 16 S L1 AND (VARIABLE (3A) SPEED (5A) CLOCK?)
L5 369 S L1 AND (SINGLE (2A) CHIP (5A) PROCESSOR?)
L6 0 S L4 AND L5
L7 289 S L1 AND (VARIABLE (5A) CLOCK?)
L8 11 S L5 AND L7

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U.S. Patent & Trademark Office

P0003

=> s 395/?/ccls

L1 35978 395/?/CCLS

=> s (cpu? (5a) clock? (5a) same (5a) chip?)/ab and l1

3187 CPU?/AB

18308 CLOCK?/AB

126218 SAME/AB

14799 CHIP?/AB

1 (CPU? (5A) CLOCK? (5A) SAME (5A) CHIP?)/AB

L2 0 (CPU? (5A) CLOCK? (5A) SAME (5A) CHIP?)/AB AND L1

=> s l1 and (cpu? (5a) clock? same (5a) chip?)

47295 CPU?

258622 CLOCK?

1584776 SAME

28 CLOCK? SAME

(CLOCK? (W) SAME)

119150 CHIP?

0 CPU? (5A) CLOCK? SAME (5A) CHIP?

L3 0 L1 AND (CPU? (5A) CLOCK? SAME (5A) CHIP?)

=> s l1 and (cpu? (5a) clock? (5a) same (5a) chip?)

47295 CPU?

258622 CLOCK?

1584776 SAME

119150 CHIP?

3 CPU? (5A) CLOCK? (5A) SAME (5A) CHIP?

L4 2 L1 AND (CPU? (5A) CLOCK? (5A) SAME (5A) CHIP?)

=> d kwic l4 1-2

US PAT NO: 5,414,862 [IMAGE AVAILABLE]

L4: 1 of 2

US-CL-CURRENT: 395/750; 364/273, 273.5, 948.4, 948.91, DIG.1, DIG.2

DETDESC:

DETD(132)

An . . . embodiment of this invention will be described. In this embodiment, A comparator, up/down counter and digital comparator as well as CPU, ROM, RAM, timer and system clock generator are fabricated on the same chip. Further, as the reference value to be compared at the comparator, analog data stored in ROM are used, or analog. . .

US PAT NO: 4,819,164 [IMAGE AVAILABLE]

L4: 2 of 2

US-CL-CURRENT: 395/556; 364/232.8, 270, 270.1, 270.2, 271, 271.1, DIG.1;
395/557, 559

DETDESC:

DETD(19)

During . . . slow clock signal can also be generated in conjunction with the Chip Enable Signal such that the rate of the clocking operation for the CPU 12 is reduced at the same time that a particular chip or peripheral

device is enabled. These chip enable signals and slow clock signals are input to a gate array network. . .

=> s (cpu? (5a) clock? (5a) same (5a) chip?)

47295 CPU?

258622 CLOCK?

1584776 SAME

119150 CHIP?

L5 3 (CPU? (5A) CLOCK? (5A) SAME (5A) CHIP?)

=> d kwic l5 1-3

US PAT NO: 5,414,862 [IMAGE AVAILABLE]

L5: 1 of 3

DETDDESC:

DETD(132)

An . . . embodiment of this invention will be described. In this embodiment, A comparator, up/down counter and digital comparator as well as CPU, ROM, RAM, timer and system clock generator are fabricated on the same chip. Further, as the reference value to be compared at the comparator, analog data stored in ROM are used, or analog. . .

US PAT NO: 5,058,116 [IMAGE AVAILABLE]

L5: 2 of 3

ABSTRACT:

A . . . and correcting technique. When a single error is detected, a cycle is inserted by the control circuitry of the cache chip. At the same time, the clocks for the CPU are held high until released by the cache chip on the next cycle. Error correction on multi-byte data is performed. . .

US PAT NO: 4,819,164 [IMAGE AVAILABLE]

L5: 3 of 3

DETDDESC:

DETD(19)

During . . . slow clock signal can also be generated in conjunction with the Chip Enable Signal such that the rate of the clocking operation for the CPU 12 is reduced at the same time that a particular chip or peripheral device is enabled. These chip enable signals and slow clock signals are input to a gate array network. . .

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